

Exercises for “Computer Science II” — SS 2003

No. 7

Due: June 27, 2003

Memory Management

1. In a typical one-level paging virtual memory system, a memory access by the CPU often takes the following steps: **(4 points)**
 - (1) Look up the physical address in the TLB. If TLB hit, go to step 4.
 - (2) Look up the physical address in the page table, which is always in memory.
 - (3) If the page table indicates a page fault, the page fault routine is called to read the page into memory.
 - (4) Read the data into some CPU register.

Suppose the TLB miss rate is p_1 , and the probability of a page fault is p_2 . Also suppose the time to read or write a value in memory is m , the time to look up the TLB is x , and the time to handle a page fault is d . What is the effective memory access time?

Input/Output Management

2. Briefly describe the steps taken to read a block of data from the disk to the memory using DMA controlled I/O. **(4 points)**
3. Polling for an I/O completion can waste a large number of CPU cycles if the processor iterates a busy waiting loop many times before the I/O completes. But if the I/O device is ready for service, polling can be much more efficient than is catching and dispatching an interrupt. Describe an algorithm that combines polling, sleeping and interrupts for I/O device service. **(4 points)**

File Systems

4. Explain what is symbolic link and list at least two of its drawbacks. **(3 points)**
5. Suppose a file system can have three disk allocation strategies, contiguous, linked and indexed. We have just read the information for a file from its parent directory. For contiguous and linked allocation, this gives the address of the first block; for indexed allocation this gives the address of the index block. Now we need to read the 10th data block into the memory. How many disk blocks do we have to read for each of the allocation strategies? **(3 points)**